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Title: **16 Lane SUPI -** An implementation of OC768 SFI-5 interface

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Abstract: A 16 x 2.5Gb electrical interface for OC768 is proposed as an implementation of SFI-5. This interface has 16 lanes of data which can have random phase relationship - a methodology for lane de-skew is described, which avoids transmitting synchronous clocks and tight timing relationships. A motion is included to move that 16 lane SUPI is adopted as baseline text for SFI-5

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16 Lane SUPI

Reference Model

- To provide an electrical interface between an OC768 Framer component and a Serdes component.
- To be compliant with OC768 as defined in ITU G707
- Interface to be configurable as quad OC192.
- Serdes component to be assembled in an Optical module or sub-assembly (daughter-board). Framer to be on main system board.
- SFI-5 interface to apply over <10" PCB track plus module connector.
- Number of board connections to be minimized.
- Interface structured to be non-critical to timing skew.
- Parallel interface to be compatible with current CMOS ASIC technologies.

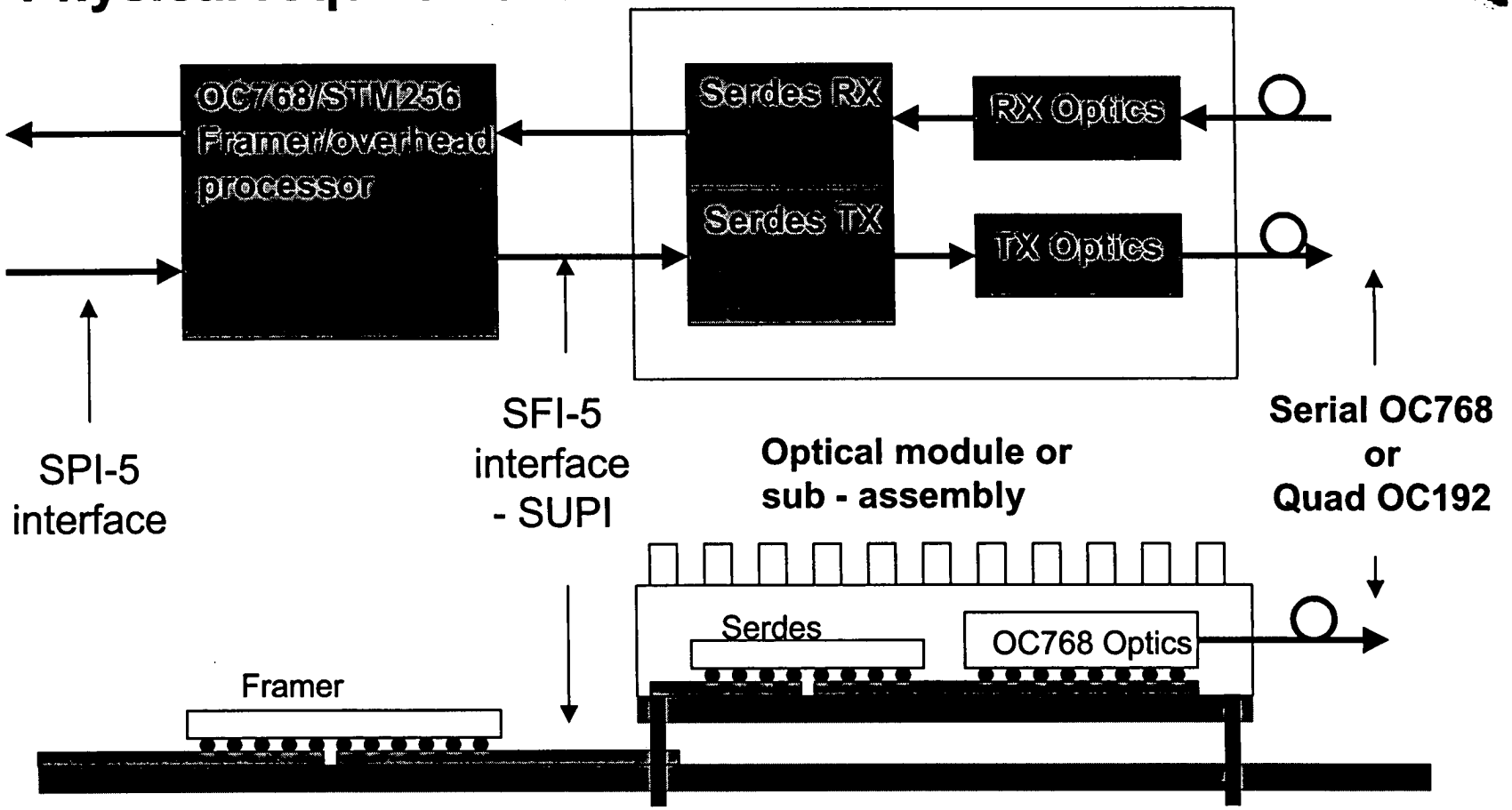
16 Lane SUPI

SUPI - Simple Universal PMD Interface

- Has been adopted by IEEE 802.3ae as a parallel interface between PCS (coding layers) and PMD (optical interface), applicable for WAN data over 4 x 2.5Gb WWDM link.
- Provides an interface for OC192 like data striped over 4 2.5Gb lanes - 16 connections on board.
- 4 lanes are equal frequency, but arbitrary phase relationship.
- Framing bytes are maintained on each lane to enable de-skew.
- No clocks transmitted - clock recovered at destination.

16 Lane SUPI

Physical requirements



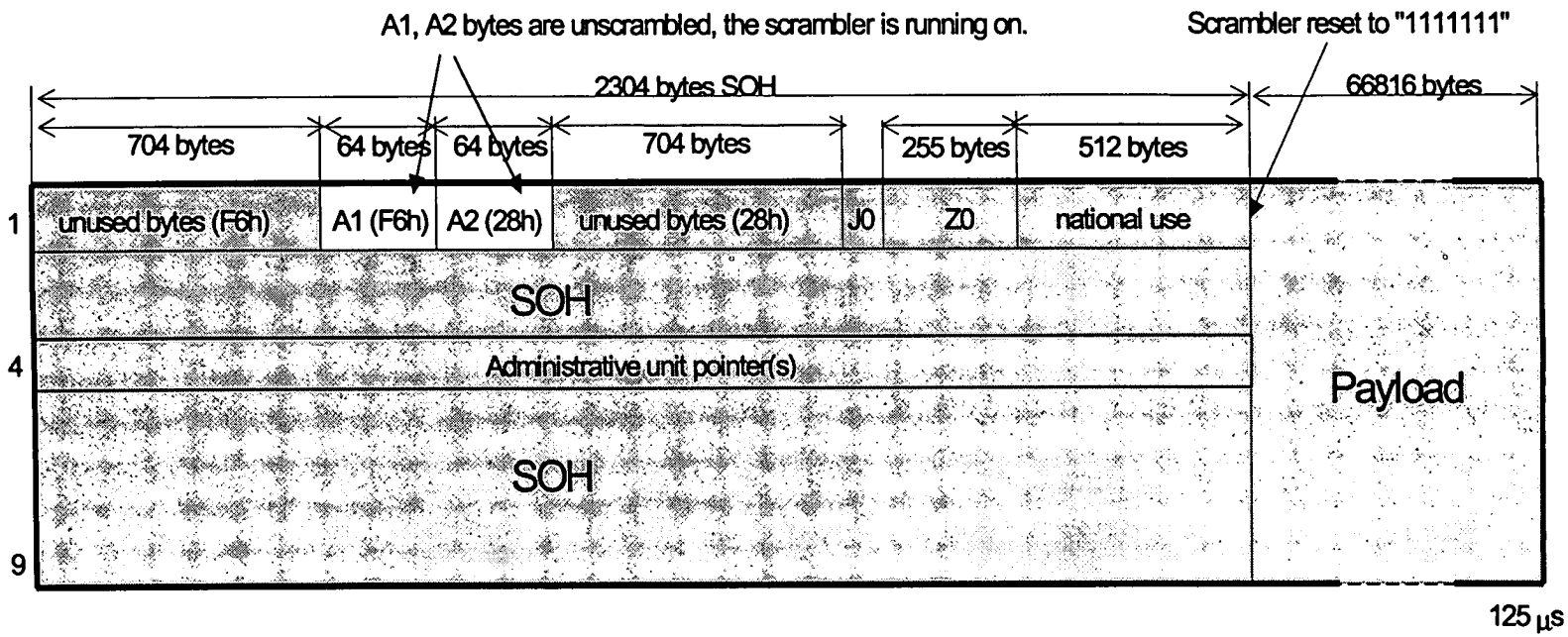
16 Lane SUPI

Summary description

- OC768 frame is demultiplexed to 16 Lanes of 2.5Gb data
- each Lane is synchronous, with potential multi-bit phase skew relationship
- each data lane to include frame bytes for de-skew
- No clocks transmitted - total of 64 board connections
- OC768 framed data stripped onto 16 2.5Gb lanes in 16 bit segments to maintain integrity of framing bytes
- A1/A2 byte transitions to be used for de-skew.
- Quad OC192 option mode - provides an interface for 4 independent, but synchronous OC192 data streams.

16 Lane SUPI

OC768/STM256 frame structure

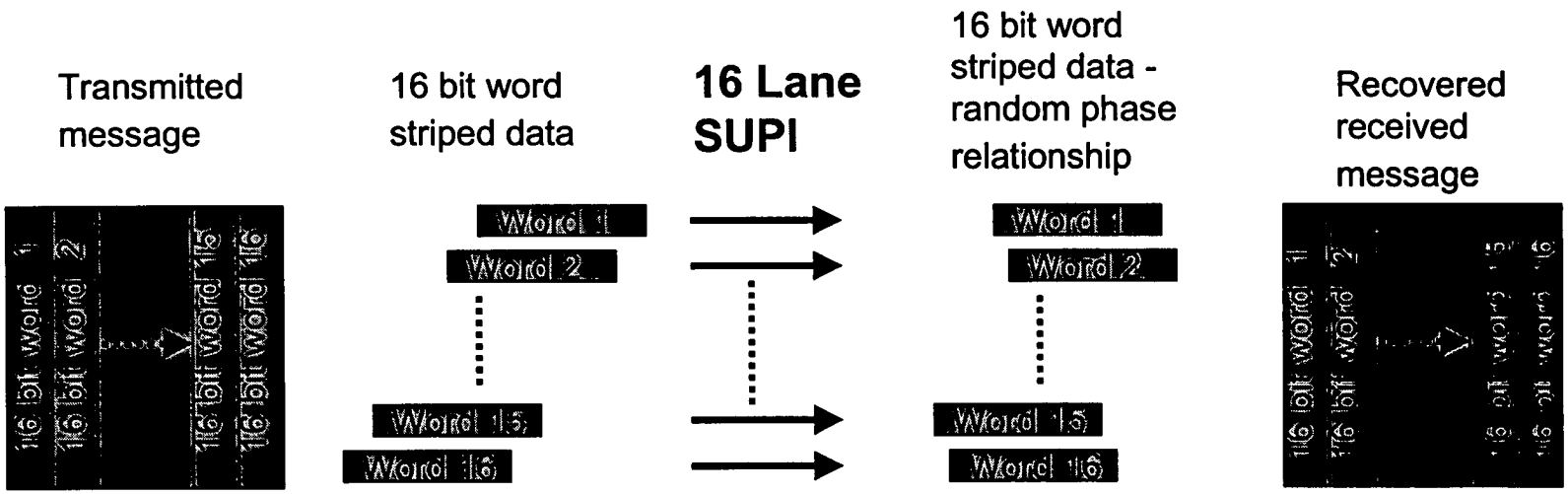


16 Lane SUPI

16 bit word striped data transmitted on each of 16 lanes

each lane has 1/16 of the A1/A2 framing bytes

– for fixed lane assignment, allows for large skew



16 Lane SUPI

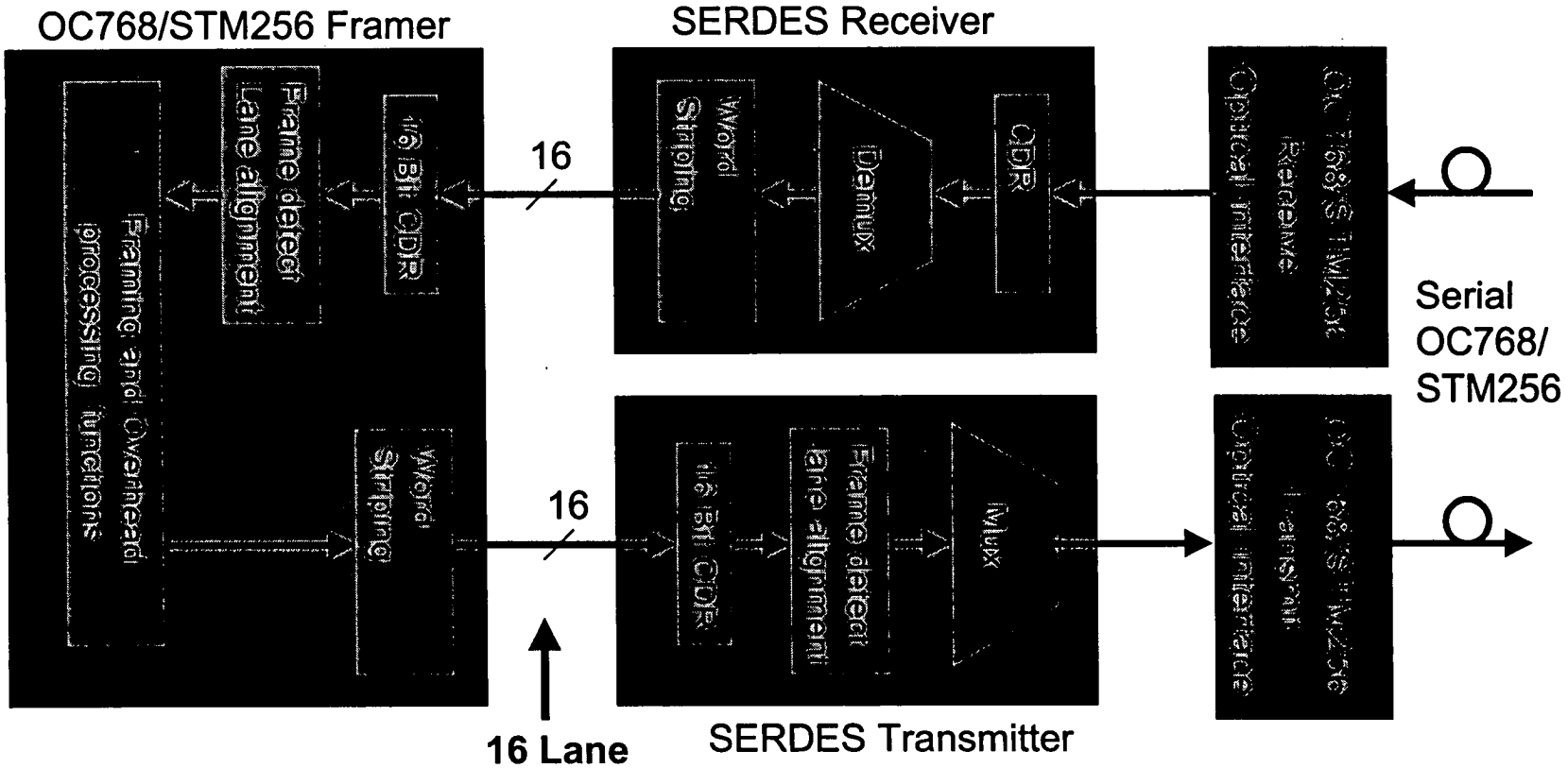
SUPI Lane de-skew

- uses A1/A2 transition (frame marker)
- looks for A1/A2 transition to achieve synchronization
  - expects it to appear on each lane every 37728 Octets
  - each lane locks onto the synchronization pattern

16 Lane SUPI

Functional implementation of 16 Lane SUPI

– OC768/STM256 mode



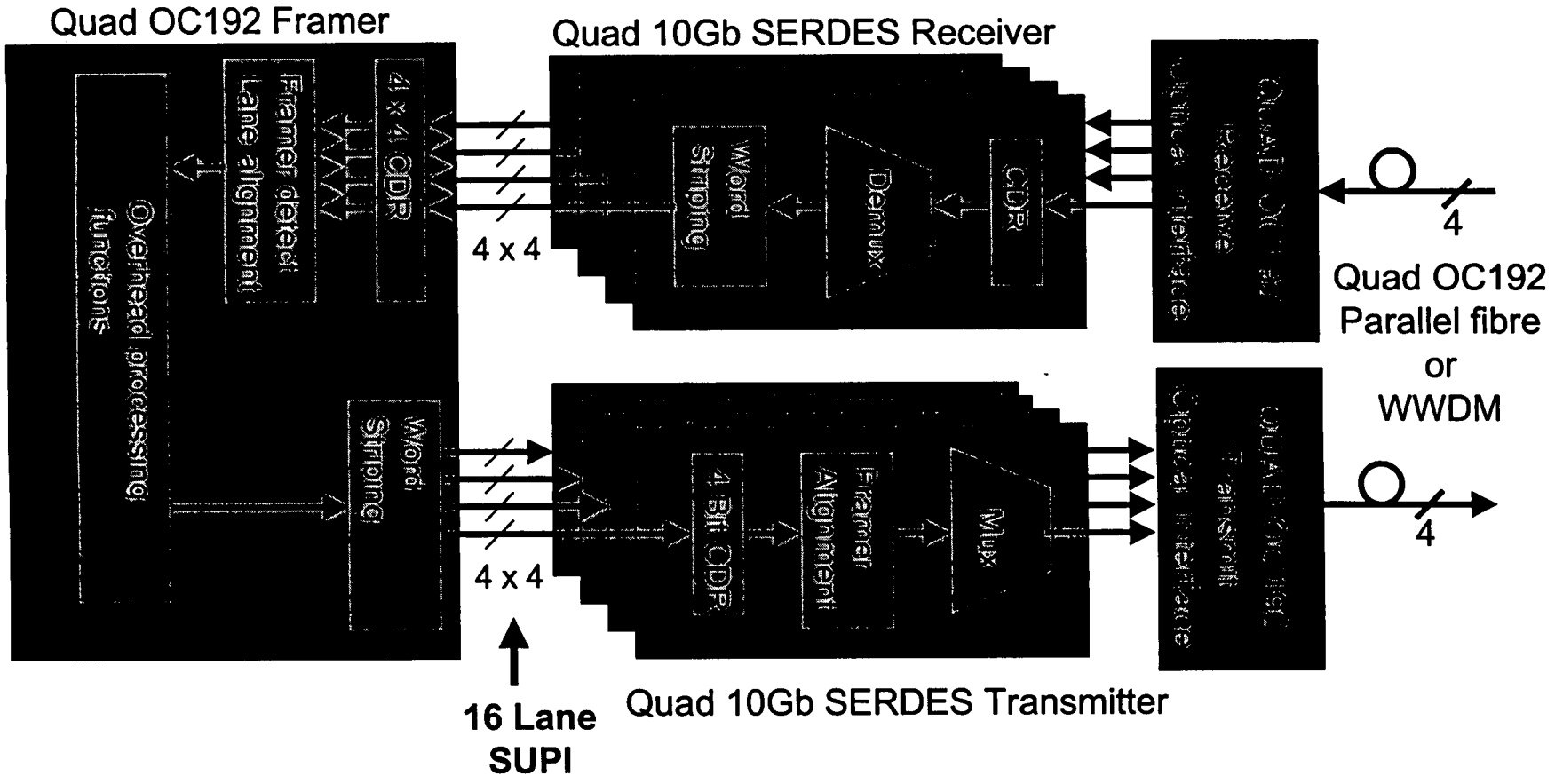
16 Lane SUPI

Implementation of Quad OC192 mode.

- OC768 can be structured as 4 independent OC192 data streams, to implement optical links as 4 x 10Gb over parallel fibre or WWDM over single fibre.
- 16 x 2.5Gb lanes structured as 4 x OC192 format.
- OC192 frame is striped across 4 x 2.5G lanes in 16 bit sections, i.e. exactly as 4 Lane SUPI in 10G Ethernet.

16 Lane SUPI

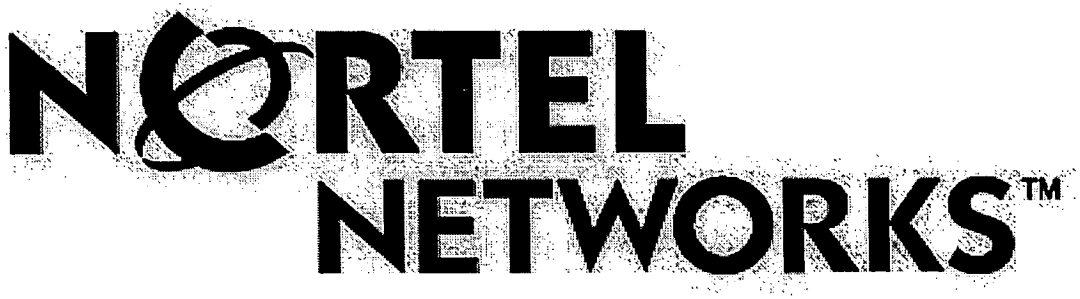
Functional implementation of Quad OC192 mode



16 Lane SUPI

- **Conclusions: A 16 Lane parallel OC768 interface is proposed which:**
  - **Simplifies PCB trace routing.**
  - **Has large lane to lane skew accommodation.**
  - **Compatible with current CMOS technology.**
  - **Eliminates timing problems associated with synchronous clocked links.**

Motion: to move that 16 Lane SUPI is adopted as the baseline text for development of the SFI-5 specification.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